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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/694,832	10/29/2003	Jaemin Lim	Q76050	9459

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EXAMINER	
BATAILLE, PIERRE MICHE	
ART UNIT	**PAPER NUMBER**
2186	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/08/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/694,832	LIM ET AL.	
	Examiner	Art Unit	
	Pierre-Michel Bataille	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 January 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) _____ is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-6 and 8-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date 10/12/06
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. The present Office Action is taken in response to applicant's communication filed January 19, 2007 responding to Non-Final Communication filed October 20, 2006. Applicant's amendment and/or arguments have been considered with the results that follow.

2. Claims 1, 3-6, and 8-11 are pending in the application under prosecution as claims 2, 7, and 12-13 have been canceled.

Response to Arguments

3. Applicant's arguments with respect to claims 1, 3-6, and 8-11 have been considered but are not deemed to be persuasive for at least the following remarks.

Applicant argues that Gibson (US 6,601,167) fails to teach:

the cache module comprises:

a cache controller that if the read operation is required by the main control unit, accesses the serial flash, reads a page to which the designated memory address belongs, and transmits data .in .the read page corresponding to the designated memory address to the main control unit;

a tag-storing unit on which storage information on the read page is written in response to an operation control of the cache controller; and

a data-storing unit on which the read page is written.

Please note that the feature noted above, allegedly not taught by Gibson features what is illustrated as "execute-in-place (XIP)" feature allowing boot loader be booted directly from UltraNAND device following power-up, i.e. the boot loader supporting UltraNAND devices temporarily becomes the source of the usual system control signal required during the boot loading program [Col. 7, Lines 38-45]. In fact Gibson teaches the feature XIP (execute-in-place) wherein an initialization process issues superset Gapless Read command to each of the UltraNAND devices to pre-load the first flash memory page, containing boot code, into the internal UltraNAND data registers allowing the system micro-controller or processor to read and execute sequential system boot code from the memory following power-up [Col. 6, Line 61 to Col. 7, Line 5]. The memory mapped base address for the UltraNAND device causes the UltraNAND device to be selected when read with a jump to the destination address for the XIP memory resource to hold the system code that was stored in UltraNAND, the UltraNAND memory contents being transferred to shadow memory [Col. 11, Line 62 to Col. 12, Line 14; Col. 7, Lines 24-35].

It is believed that all features of the claims are taught either explicitly or implicitly by Gibson and the rejection is maintained and repeated below.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1, 3-6, and 8-11 are rejected under 35 U.S.C. 102(e) as being anticipated by US 6,601,167 (Gibson et al).

With respect to claims 1, 6, and 8, Gibson discloses the invention as claimed, an apparatus having a flash memory chip and method for controlling execute-in-place (XIP) in a serial flash, comprising:

a cache module for accessing a designated memory address of the serial flash in response to a command received from a main control unit through a system interface unit, and reading or writing data required by the main control unit in a read or write operation ***(execute-in-place volatile random access memory or alternative cache or other memory in processor) [Col. 5, Lines 14-19]***;

a serial flash controller comprising a boot loader for allowing system booting to be performed by reading boot codes written on the serial flash ***(logic circuitry of sequential access memory 32 required for performing boot***

loader function) [Fig. 8; Col. 6, Lines 2-8], storing the boot codes in a buffer and immediately transmitting the boot codes to the main control unit when the main control unit requires the boot codes **(boot code copied from sequential access memory 32 to execute-in-place volatile random access memory upon initialization of the computer system) [Col. 6, Lines 53-67; Col. 5, Lines 13-19]**; and

a flash interface unit for handling transmission and reception of data among the cache module, the serial flash controller and the serial flash **(micro-controller based systems generally have Programmable Input/Output (PIO) pins available which can be used to directly provide the UltraNAND control signals or some additional interface logic required for an appropriate connection between the processor, boot loader and sequential memory) [Col. 6, Lines 23-28]**;

the cache module comprising:

a cache controller that if read operation is required by main control unit access the serial flash, read a page to which the desired memory address belongs and transmits data in the read page corresponding to the designated memory address to the main control unit ***(general principle of cache memory as cache memory is used to temporary storage to make data available at fast pace)*** **Gibson discloses gapless read enabled reading code from cache memory at determined address page location [Col. 3, line 52 to col. 4, Line 34]**;

tag storing unit on which storage information on the read page is written in response to an operation control of the cache controller; and a data storing unit on which the read page is written **(general principle of cache memory as most cache memories have a data storage unit section and a tag storage unit section, the data storage unit section for storing the data and the tag storage unit section for storing tag information related to the data) Gibson discloses gapless read enabled reading code from cache memory at determined address page location [Col. 3, line 52 to col. 4, Line 34].**

With respect to claims 3-5, 9-11, Gibson discloses the boot program being configured to anticipate the behavior of any code prefetching logic and ensure that data expected to be required by the control unit is stored in the buffer [Table 2 & 3; Col. 12, Lines 33-44; Col. 13, Lines 7-13]. Gigson discloses that many processors have an instruction fetch state machine that reads instructions into a buffer ahead of the actual use of instructions by the instruction execution state machine of the processor [Col. 4, Lines 46-49].

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

US 6,948,099 Tallam) teaching the ability to recover from corruption by including boot code on Flash memory device.

7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Pierre-Michel Bataille whose telephone number is (571) 272-4178. The examiner can normally be reached on Mon, Tue-Fri (8:00A to 5:30P).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew M. Kim can be reached on (571) 272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Pierre-Michel Bataille
Primary Examiner
Art Unit 2186